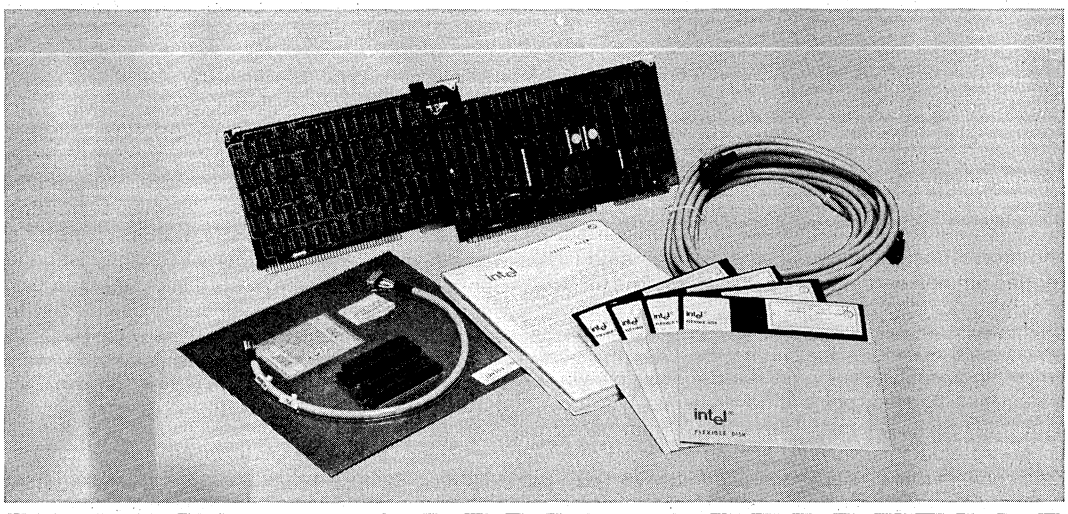
MODEL 677 DS/E ETHERNET* UPGRADE KIT FOR INTELLEC® DEVELOPMENT SYSTEMS

- **Complies with the Intel®, DEC, and Xerox Tricompany Ethernet Specification**
- **Includes an Ethernet Data Link Layer Software Library to allow user programs to access the Ethernet Data Link from the 8085 in Series II and Series III**
- **Supports the Ethernet Data Link and Physical Link Control over the MULTIBUS**
- **Includes a special 10 meter Interconnect Cable for connecting two DS/E units for Ethernet software prototyping**
- **Upgrades Intellec® Series II/85 and Series III Development Systems**

The DS/E Ethernet Upgrade Kit provides the Series II/85 or Series III user with the additional tools necessary to develop and test communication software and applications that will use Ethernet as a communication subsystem. It combines the power of the Intellec Microcomputer Development System with its dual board Ethernet Communications Controller for microprocessor development. This combination allows the user to develop either 8- or 16-bit Ethernet-based applications.

The Ethernet Communications Controller incorporates the Ethernet Data Link and Physical Link Control to meet the Ethernet specification for 10 Mbit per second data transmission rate over coaxial cable. The controller consists of two MULTIBUS compatible boards, the Processor board and the Serialization/Deserialization (SerDes) board. The Processor board provides the function of packet buffering, processing, and transferring of the processed packets to system memory. The SerDes board performs the serialization/deserialization, framing, CRC generation and checking, Manchester encoding/decoding, and destination address recognition. A 10 meter interconnect cable is included to permit two DS/E units to be connected in a functioning Ethernet environment without the need for Ethernet transceivers and coaxial cable.

*Ethernet is a trademark of Xerox Corporation.



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Ethernet Communications Controller

PROCESSOR BOARD

The processor board interfaces to the MULTIBUS system bus and contains the Intel 5 MHz 8088 CPU, 16 Kbytes dynamic RAM for Ethernet and host interface program execution, 8K EPROM pre-programmed for the Data Link Control, and an 8K static RAM for transmit and receive channel DMA data buffering. The Processor board provides the necessary commands and control to the SerDes board and receives status and data from it.

SerDes BOARD

The SerDes board meets the required electrical specification to the transceiver and provides the Data Link Layer of the Ethernet architecture. The major functions of the SerDes board include serialization/deserialization, framing, Manchester encoding/decoding, transmit data flow control, receive data flow control, destination address decoding for received message, CRC generation and checking, and diagnostic for CRC error, loop-back, transmit timeout, and if used with transceivers, CSMA/CD (carrier-sense multiple-access with collision-detection).

DATA BUFFERING

All data transfers from the Ethernet Data Link control of the SerDes board are buffered through the 8K static RAM. This minimizes the amount of bus time used by the Ethernet Communications Controller by eliminating the possibility of data overruns and subsequent repeated I/O operations. In addition, the buffer allows the Ethernet Communications Controller to have a bus priority below higher-priority, time-critical parts of the system.

DIAGNOSTICS

Diagnostic functions are resident on the SerDes board and can be invoked on demand by the program on the Processor board. These functions incude: transmitting packets with a bad CRC; receiving all packets regardless of address; reading data received in error; SerDes loop-back, this function allows data from static RAM to be transmitted and received simultaneously (the received data is verified but not written to the Static RAM). The CRC generation and checking can be used to verify transmit and receive data.

When the 10 meter interconnect cable between two DS/E Units is used, point-to-point diagnostics are available to verify station-to-station communications, cable data sensitivity, CRC, packet length errors, and external carrier sense. In addition to these functions, a loop-back diagnostic is provided for use with transceivers. This function is similar to the SerDes loop-back diagnostic except the transceiver cable is also verified.

Figure 1 is a block diagram of the Ethernet Communications Controller.

Software

Three levels of program interface are provided to users of the Model 675 for Ethernet software prototyping and evaluation.

MULTIBUS MESSAGE EXCHANGE (MMX)-ISIS-II

MULTIBUS Message Exchange (MMX)-ISIS-II is a simple processor-to-processor protocol which permits ISIS-II user programs to communicate with the software residing on the Ethernet Communications Controller.

The model of use of MMX is as follows: The calling program will allocate a segment of memory in the 64 Kbyte segment accessible by ISIS-II, fill in application defined fields, and transmit via MMX to a socket on the Ethernet Communications Controller. The program then waits for the application level response to the command just given. There is an MMX module in ROM on the Ethernet Communications Controller, and another in the HOST RAM.

EXTERNAL DATA LINK (EDL)

The External Data Link (EDL) presents a subset of the Data Link Layer interface to users at the MMX-ISIS-II interface level. This allows a user to write Ethernet application programs to access the Ethernet Data Link on the 8085A-2 in ISIS-II systems. The External Data Link resides in the ROM on the Ethernet Communications Controller.

ETHERNET DATA LINK LIBRARY

The Ethernet Data Link Library is provided to simplify the External Data Link (EDL), MMX-ISIS-II interface. This library provides synchronous interface procedures for the EDL functions. These procedures allow the user to simply call a subroutine without being aware of the MMX-ISIS-II transaction which is made with the Ethernet Communications Controller. The Ethernet Data Link Library is provided on a diskette. It is designed to be linked with the user's software residing in the HOST RAM.

About the Ethernet

The Ethernet local area network provides a communication facility for high speed data exchange among digital devices located within a moderate

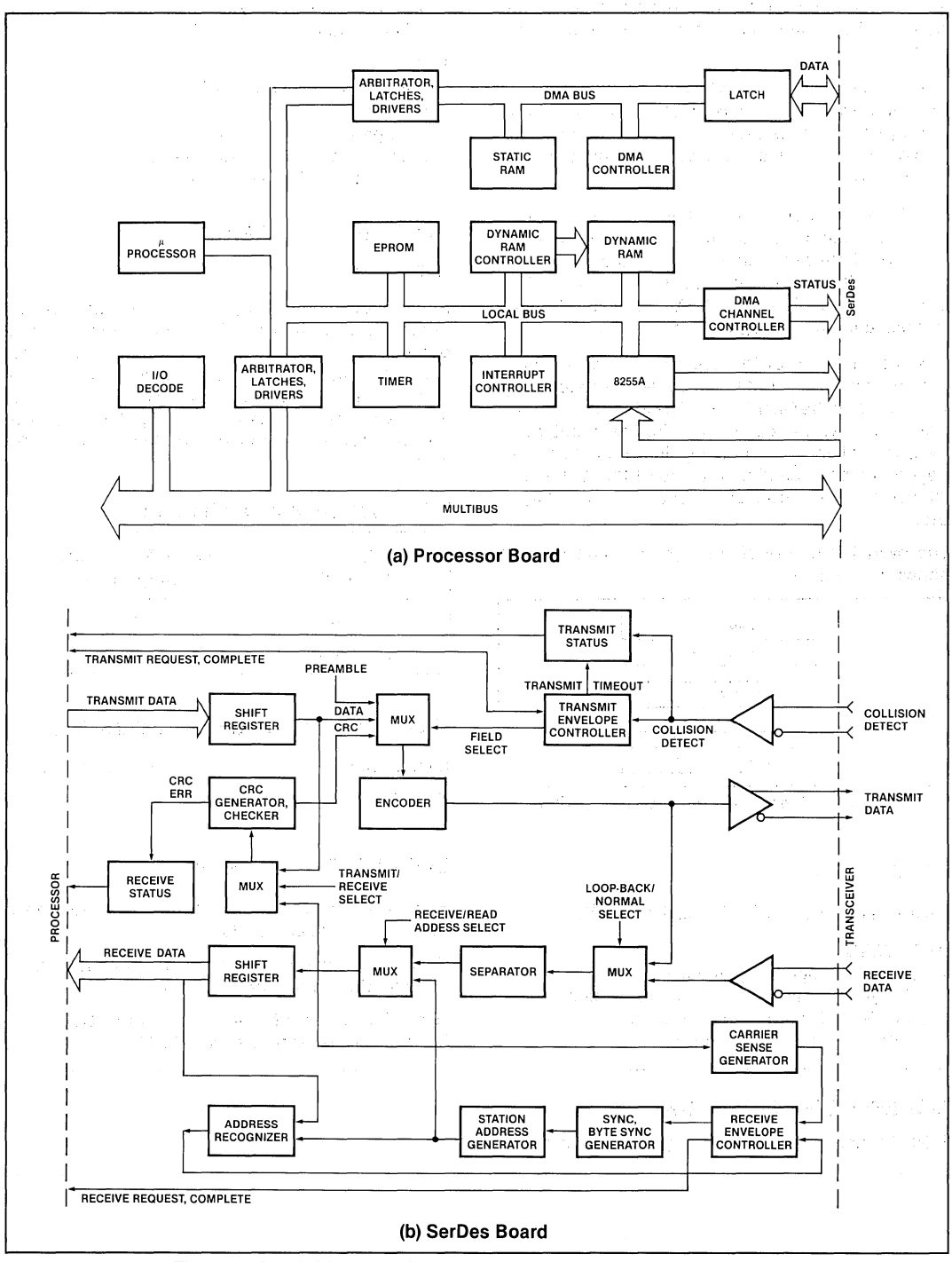

Figure 1. Block Diagram of the Ethernet Communications Controller

sized geographic area. The Ethernet architecture defines the system as a series of independent layers.

The lowest layer, the Physical Link Layer, is concerned with the coaxial cable interface. It completely specifies the essential physical characteristics of the Ethernet, such as data encoding, timing, and voltage levels.

The Data Link defines a medium-independent link level communication facility, built on the medium-dependent physical channel provided by the Physical Layer. It supports the peer protocol statistical contention resolution (CSMA/CD), variable size frames, and link management functions.

The higher levels of the overall network architecture, which use the Data Link Layer, are collectively referred to as the Client Layer. The identity and function of this layer are user specific. The intent, however, is that the Ethernet Physical and Data Link Layers support the higher layers of the ISO model (Network Layer, Transport Layer, Session Layer, etc.).

The overall structure of the layered architecture is shown in Figure 2.

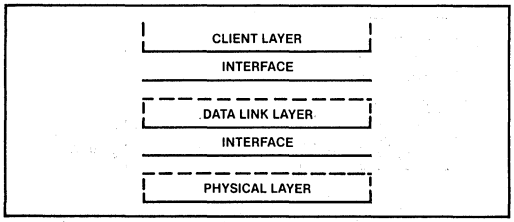

Figure 2. Ethernet Architectural Layering

SPECIFICATIONS

Ethernet Communications Controller

PROCESSOR
—8088 based, operating at 5 MHz
—16K dynamic RAM for program execution
—8K EPROM for program execution
—8K Static RAM for data buffer
—3 DMA channels for receive data
—1 DMA channel for transmit data

SerDes
—Serialization/Deserialization
—Framing
—CRC generation and checking
—Manchester encoding/decoding
—Destination address recognition

ELECTRICAL CHARACTERISTICS

DS677 Kit

Ethernet Development Upgrade Kit includes the Ethernet Communication Controller board set (2 boards), top assembly hardware, 10m interconnect cable, data link interface library, diagnostic test programs, manuals and documentation. Will give Ethernet development capability to any Series II/85 or Series III development system. (Shipping weight 10.5 lbs.)

DC Power Supply for Mainframe

Volts Supplied	Current Requirements Amps Max.
+5±5%	9.0
+12±5%	0.5

ENVIRONMENTAL CHARACTERISTICS

System Operating Temperature—16°C to 32°C (61°F to 90°F)
Humidity—20% to 80%

DOCUMENTATION SUPPLIED

Ethernet Communications Controller Programmer's Reference Manual, 121769.

Ethernet Development System Upgrade Kit Installation and Checkout Manual, 121778.

iSBC-550 Ethernet Communications Controller Hardware Reference Manual 121746.

ORDERING INFORMATION

DS677 Ethernet Upgrade Kit requires a Software License.